

REMARKS

Claims 2, 3, 5-10, 26, 27, 29-34, 36 and 39-44 are pending. In the Office Action dated December 21, 2009 the Examiner rejected claims 2, 3, 5-10, 26, 27, 29-34, 36 and 39-44 on the ground of nonstatutory obviousness-type double patenting, as being unpatentable over claims 1-17 of U.S. Patent No. 7,518,422 to Johnson.

Because 35 U.S.C. § 121 prohibits a double patenting rejection in this situation, Applicant respectfully traverses the rejection of claims 2, 3, 5-10, 26, 27, 29-34, 36 and 39-44 and requests the rejection be reconsidered and withdrawn.

35 U.S.C. § 121 states in part that "A patent issuing on an application with respect to which a requirement for restriction ... has been made ... shall not be used as a reference ... against a divisional application." U.S. Patent No. 7,518,722 issued on an application which is a divisional of the present application. Accordingly, a non-obviousness-type double patenting rejection is inappropriate. *See* MPEP 804.01.

A restriction requirement issued by the Office on June 23, 2005 required imposed a two-way restriction requirement between Group 1, characterized by the Examiner as directed toward a memory circuit, and Group 2, characterized by the Examiner as directed toward a delay locked loop circuit. *See* Restriction Requirement, June 23, 2005.

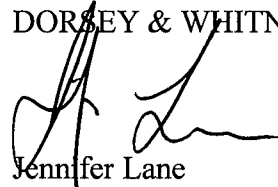
Responsive to the restriction requirement, Applicant elected Group 1, and filed a divisional application directed to the claims of Group 2, which application has since issued as U.S. Patent No. 7,518,422. The claims of Group 1 were, at the time of restriction, directed toward device and system board claims. *See* Originally-filed claims 1-10 and 25-44, December 11, 2003. The allowed Group 1 claims above continue to be directed toward devices and system boards. The claims of Group 2 were, at the time of restriction, directed toward phase-locked loop and method claims. *See* Originally filed claims 11-24 and 45-49, December 11, 2003. The issued Group 2 claims in U.S. Patent 7,518,722 are directed toward delay locked loops, circuits, and methods.

Having imposed a restriction requirement in the application family, the Office is prohibited by 35 U.S.C. § 121 from now issuing a double-patenting rejection between very groups of claims that were subject to the restriction. Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Applicant respectfully submits the application is in condition for allowance.
Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP

A handwritten signature in black ink, appearing to read "Jennifer Lane", is written over the printed name.

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